C. Amendments to the Claims.

1. **(Currently Amended)** A method of forming a plurality of semiconductor device layers, comprising the steps of:

forming an oxide layer on an exposed surface of an insulating layer **comprising silicon and nitrogen** by reacting hydrogen with oxygen on the exposed surface of the insulating layer deposited over a wafer; and

forming a conductive gate layer over the oxide layer.

2. (Previously Amended) The method of claim 1, wherein:

the reacting of hydrogen with oxygen is performed at a wafer temperature in the range of about 800°C to 1300°C.

3. (Original) The method of claim 1, wherein:

the oxide layer has a thickness in the range of 20-60 angstroms.

4. (Previously Amended) The method of claim 1, wherein:

the reacting of hydrogen with oxygen on the wafer surface has a duration in the range of 30 seconds to 2 minutes.

5. (Previously Amended) The method of claim 4, wherein:

the reacting of hydrogen with oxygen on the wafer surface has a duration in the range of approximately 1 minute.

6. (Original) The method of claim 1, wherein:

the conductive gate material includes polysilicon.

7. (Original) The method of claim 1, wherein:

the oxide layer and conductive gate layer form a SONOS-type device.

8. (Original) The method of claim 1 wherein steps prior to forming the oxide layer comprise:

forming a tunnel dielectric; and

depositing the insulating layer, the insulating layer being a charge storing dielectric layer.

9. (Original) The method of claim 8, wherein:

the charge storing dielectric layer includes silicon nitride.

10. (Original) The method of claim 1, further including:

forming a gate etch mask; and

etching to form gate stacks; and

forming insulating sidewalls on the gate stacks.

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11. (Original) The method of claim 8, wherein:

forming the tunnel dielectric, forming the charge storing dielectric layer, and forming the oxide layer occur in a single wafer processing tool.

12. **(Currently Amended)** A method, comprising the steps of:

forming a bottom dielectric on a substrate surface;

forming a middle dielectric over the bottom dielectric; and

forming a top dielectric over the middle dielectric by heating the substrate to less than about 1200°C for less than two minutes <u>and reacting a hydrogen containing source gas with an oxygen containing source gas on the surface of the middle dielectric</u>.

13. **(Cancelled)** The method of claim 12, wherein:

forming the top dielectric further includes reacting the surface of the middle dielectric layer with hydrogen (H_2) and oxygen (O_2).

14. (Original) The method of claim 12, wherein:

the middle dielectric comprises at least one layer selected from the group consisting of silicon nitride, silicon oxynitride, and silicon rich silicon nitride.

15. (Original) The method of claim 12, wherein:

the bottom dielectric has a thickness of less than 15 angstroms; and

the top dielectric has a thickness of less than 50 angstroms.

16. (Original) A method of manufacturing a SONOS-type device, comprising the steps of:

oxidizing a charge storing dielectric comprising at least one layer that includes silicon and nitrogen by reacting hydrogen with oxygen to form a top oxide layer over the charge storing dielectric.

17. (Original) The method of claim 16, wherein:

the oxidizing lasts for less than two minutes.

18. (Original) The method of claim 16, wherein:

the oxidizing occurs at a temperature of less than 1200°C.

19. (Original) The method of claim 16, further including:

a tunnel dielectric formed below the charge storing dielectric;

forming a conductive gate layer over the top oxide layer; and

patterning at least the top oxide and charge storing dielectric to form a gate stack.

20. (Currently Amended) The method of claim 196, ~~wherein~~ further including:

forming the tunnel dielectric, forming the top oxide layer, and forming the top dielectric in the same wafer processing tool~~has a thickness greater than 20 angstroms~~.

21. (New) The method of claim 8, further including:

forming the bottom dielectric, the middle dielectric and the top dielectric in the same wafer processing tool.